KSHITIJ BHARDWAJ

CONTACT INFORMATION

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RESEARCH INTERESTS

Heterogeneous systems-on-chip (SoCs) for artificial intelligence (AI) applications, GALS (globally-asynchronous locally-synchronous) systems, asynchronous circuits, hardware accelerator design, system-level design and optimization, networks-on-chip (NoCs), and computer-aided design (CAD) for VLSI.

EDUCATION

Columbia University, New York, NY

Ph.D., Computer Science (2018)
Advisor: Prof. Steven M. Nowick
Dissertation: On Multicast in Asynchronous Networks-on-Chip: Techniques, Architectures, and FPGA Implementation

Utah State University, Logan, UT

M.S., Computer Engineering (2012)
Advisor: Prof. Koushik Chakraborty
Thesis: Aging-Aware Routing Algorithms for Networks-on-Chip

Devi Ahilya University, Indore, MP, India

Bachelor of Engineering, Electronics & Instrumentation (2010)

HONORS AND AWARDS

- **Outstanding Graduate Research Assistant** (2011-2012), Electrical and Computer Engineering Department, Utah State University, Logan, UT
- Award from **Young Student Support Program**, Design Automation Conference (DAC) 2012

PROFESSIONAL EXPERIENCE

John A. Paulson School of Engineering and Applied Sciences
Harvard University, Cambridge, MA

- **Post-Doctoral Research Fellow** (2018 - current)
  Post-doc advisors: Prof. David Brooks and Prof. Gu-Yeon Wei

Department of Computer Science
Columbia University, New York, NY

- **Graduate Research Assistant** (2012 - 2018)
  Advisor: Prof. Steven M. Nowick.

Intel Corporation: Intel Labs
Hillsboro, OR

- **Graduate Technical Intern: High Performance Circuits Lab** (July-Oct 2016)

Cadence Design Systems
San Jose, CA

- **Software Engineer Intern: Emulator Design and Verification Group** (May-Aug 2015)

Department of Electrical and Computer Engineering
Utah State University, Logan, UT

- **Graduate Research Assistant** (2010 - 2012)
  Advisor: Prof. Koushik Chakraborty

Patents

- **Global and Local Time-Step Determination Schemes for Neural Networks**, Gregory Chen (Intel), Kshitij Bhardwaj, Raghavan Kumar (Intel), Huseyin Sumbul (Intel), Phil Knag (Intel), Ram Krishnamurthy (Intel), Himanshu Kaul (Intel), US Patent Application: 2019/0102669 (Published: April, 2019).
- **Aging-Aware Routing for NoCs**, Kshitij Bhardwaj, Koushik Chakraborty (USU), Sanghamitra Roy (USU), US Patent: 9,344,358 (May 17, 2016).

Papers Under Submission or Preparation

1. Sam Xi, Yuan Yao, **Kshitij Bhardwaj,** Paul Whatmough, David M. Brooks, and Gu-Yeon Wei. *SMAUG: end-to-end full-stack simulation infrastructure for deep learning workloads.* Under submission in International Symposium on Computer Architecture (ISCA), 2020.
2. Davide Bertozzi, Gabriele Miorandi, Alberto Ghiribaldi, Wayne Burleson, Greg Sadowski, **Kshitij Bhardwaj,** Weiwei Jiang, and Steven M. Nowick. *Cost-effective and flexible asynchronous interconnect technology for GALS systems.* Under submission in IEEE Micro Magazine.
3. Srivatsan Krishnan, **Kshitij Bhardwaj,** Zishen Wan, Paul Whatmough, David M. Brooks, Gu-Yeon Wei, and Vijay J. Reddi. *AutoPilot: automating algorithm-system co-design for aerial autonomous robots.* To be submitted in International Symposium on Microarchitecture (MICRO), 2020.

Journal Publications

1. **Kshitij Bhardwaj,** Marton Havasi, Yuan Yao, David M. Brooks, Jose Miguel Hernandez Lobato, and Gu-Yeon Wei. *Determining optimal coherency interface for many-accelerator SoCs using Bayesian optimization.* In IEEE Computer Architecture Letters (CAL), Sept 2019, vol. 18, no. 2, pp. 119-123.
2. **Kshitij Bhardwaj** and Steven M. Nowick. *A continuous-time replication strategy for efficient multicast in asynchronous NoCs.* In IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Feb 2019, vol. 23, no.2, pp. 350-363.
3. Dean Ancajas, **Kshitij Bhardwaj**, Koushik Chakraborty and Sanghamitra Roy. *Wearout resilience in NoCs through an aging aware adaptive routing algorithm.* In IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Feb 2015, vol.23, no.2, pp. 369-373.

Conference Publications

1. **Kshitij Bhardwaj,** Paolo Mantovani, Luca Carloni, and Steven M. Nowick. *Towards a complete methodology for synthesizing bundled-data asynchronous circuits on FPGAs.* Proceedings of International Symposium on Low Power Electronics and Design (ISLPED 2019), Lausanne, Switzerland, pp. 1-6.
2. **Kshitij Bhardwaj,** Weiwei Jiang and Steven M.Nowick. *Achieving lightweight multicast in asynchronous NoCs using a continuous-time multi-way read buffer.* Proceedings of International Symposium on Networks-on-Chip (NOCS 2017), Seoul, South Korea, pp. 1-8 **(Best paper nomination)**.
3. **Kshitij Bhardwaj** and Steven M. Nowick. *Achieving lightweight multicast in asynchronous networks-on-chip using local speculation.* Proceedings of Design Automation Conference (DAC 2016), Austin, Texas, pp. 38:1-38:6.
4. Weiwei Jiang, **Kshitij Bhardwaj,** Geoffray Lacourba and Steven M. Nowick. *A lightweight early arbitration method for low-latency asynchronous 2D-mesh NoC's.* Proceedings of Design Automation Conference (DAC 2015), San Francisco, CA, pp. 203:1-203:6.

5. **Kshitij Bhardwaj,** Koushik Chakraborty and Sanghamitra Roy. *Towards graceful aging degradation in NoCs through an adaptive routing algorithm.* Proceedings of Design Automation Conference (DAC 2012), San Francisco, CA, pp. 382-391.
6. **Kshitij Bhardwaj,** Koushik Chakraborty and Sanghamitra Roy. *An MILP-Based aging aware routing algorithm for NoCs.* Proceedings of Design, Automation & Test in Europe (DATE 2012), Dresden, Germany, pp. 326-331.
7. **Kshitij Bhardwaj,** Sanghamitra Roy and Koushik Chakraborty. *Power-Performance yield optimization for MPSoCs using MILP.* Proceedings of International Symposium on Quality Electronic Design (ISQED 2012), Santa Clara, CA, pp. 764-771.
8. **Kshitij Bhardwaj** and Rabindra K. Jena. *Energy and bandwidth aware mapping of IPs onto regular NoC architectures using multi-objective genetic algorithms.* Proceedings of International Symposium on System-on-Chips (ISSoC 2009), Tampere, Finland, pp. 27-31.
9. **Kshitij Bhardwaj** and S.S. Rajput. *1.5V high performance OP AMP using self cascode structure.* Proceedings of Student Conference on Research and Development (SCOReD 2009), UPM Serdang, pp. 254-257.

Technical Program Committee Member

- IEEE/ACM Design Automation Conference (DAC), 2020
- IEEE/ACM Design Automation Conference (DAC) Late Breaking Results (LBR), 2020
- IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2020

Professional Service: Conference/Journal Reviewer

- Journal of Parallel and Distributed Computing (JPDC), 2020
- IEEE/ACM International Symposium of Microarchitecture (MICRO), 2019 (external reviewer)
- ACM Journal on Emerging Technologies in Computing Systems, 2018
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016
- ACM/IEEE Design, Automation and Test in Europe (DATE) conference, 2016 (external reviewer)
- ACM/IEEE Design, Automation and Test in Europe (DATE) conference , 2014 (external reviewer)
- IEEE International Symposium on Quality Electronic Design (ISQED) conference, 2012 (external reviewer)

Teaching Experience

Department of Computer Science
Columbia University, New York, NY

Teaching Assistant

CAD of Digital Systems (CSEE 6861), Spring 2016
- Topics include: exact and heuristics for 2-level logic minimization, multi-level logic optimization using algebraic techniques, technology mapping to target area, delay and power, tree-based covering, Boolean matching using reduced ordered binary decision diagrams (ROBDDs), system-level optimization using retiming, circuit partitioning using Kernighan-Lin algorithm, optimal resource allocation and scheduling techniques (time-constrained, force-directed), satisfiability (SAT) solvers and their applications.

Advanced Logic Design (CSEE 4823), Spring 2015
- Helped students with fundamentals of advanced topics in digital design: finite state machine synthesis and optimization, high-speed arithmetic circuits (conditional sum adder, carry-lookahead adder, parallel prefix adders), register-transfer level (RTL) methodology, low-power

techniques (sequential precomputation, bus encoding), and fault tolerance (Hamming codes, CRC codes). Modeling and simulation using VHDL.

Computer Hardware Design (EECS 4340), Fall 2014

- Helped students with topics in hardware design and synthesis: application specific integrated circuits (ASICs), SystemVerilog for design and verification, and physical design and synthesis methodologies. Introduction to Synopsys logic synthesis tools such as Design Compiler, Memory Compiler and IC Compiler.

Talks

- SRC Techcon, Austin, TX: *A Bayesian optimization-based efficient design space exploration framework for many-accelerator SoCs,* September 2019.
- Arm Research Summit, Austin, TX (Poster): *A Bayesian optimization-based design space exploration framework for many-accelerator SoCs,* September 2019.
- International Symposium on Low-Power Electronics and Design (ISLPED), Lausanne, Switzerland: *Towards a complete methodology for synthesizing bundled-Data asynchronous circuits on FPGAs,* July 2019.
- International Symposium on Networks-on-Chip (NOCS), Seoul, South Korea: *Achieving lightweight multicast in asynchronous NoCs using a continuous-time multi-way read buffer,* October 2017.
- Data Science Day, Data Science Institute, Columbia University, New York, NY (Poster): *Achieving lightweight multicast in asynchronous networks-on-chip using local speculation,* April 2017.
- Intel Circuits Research Lab, Hillsboro, OR: *Wave sorting asynchronous network-on-chip for event-driven spiking neural networks,* October 2016.
- Design Automation Conference (DAC), Austin, TX: *Achieving lightweight multicast in asynchronous networks-on-chip using local speculation,* June 2016.
- Design Automation Conference (DAC), San Francisco, CA (Poster): *Towards graceful aging degradation in NoCs through an adaptive routing algorithm,* June 2012.
- Design, Automation and Test in Europe (DATE), Dresden, Germany: *An MILP-based aging-aware routing algorithm for NoCs,* March 2012.
- Microelectronics Group, Technische Universitat, Darmstadt, Germany (Invited Talk): *An MILP-based aging-aware routing algorithm for NoCs,* March 2012.

References

- David Brooks
  Haley Family Professor, Dept. of Computer Science, Harvard University, Cambridge, MA
  email: dbrooks@eecs.harvard.edu
- Gu-Yeon Wei
  Gordon McKay Professor, Dept. of Electrical Engineering, Harvard University, Cambridge, MA
  email: gywei@g.harvard.edu
- Steven M. Nowick
  Professor Emeritus, Dept. of Computer Science, Columbia University, New York, NY
  email: nowick@cs.columbia.edu
- Luca Carloni
  Professor, Dept. of Computer Science, Columbia University, New York, NY
  email: luca@cs.columbia.edu
- Michael Kishinevsky
  Senior Principal Engineer, Strategic CAD Labs, Intel Labs, Hillsboro, OR
  email: michael.kishinevsky@intel.com